V-Band High-Efficiency Monolithic Pseudomorphic HEMT Power Amplifiers

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Abstract—**V-band monolithic power amplifiers have been developed and have demonstrated state-of-the-art performance. For the single-stage MMIC amplifier employing a 200-μm pseudomorphic HEMT, 151.4 mW (757 mW/mm) output power with 26.4% power-added efficiency at 60 GHz is achieved. Maximum power-added efficiency of 30.6% at 130-mW output power was also obtained. A three-stage MMIC amplifier utilizing the same devices demonstrated 80-mW output power, 20.5% power-added efficiency, and 17-dB associated gain at 57 GHz. The linear gain of the amplifier was 21.5 dB.**

I. Introduction

The need to develop V-band power amplifiers for use in inter satellite link, phased-array, space borne radar, and electronic warfare systems is rapidly increasing. At the same time, the approach employed must reduce the cost, size, and weight of the system; therefore, monolithic techniques are essential.

Progress in GaAs technology has led to the development of millimeter-wave power HEMT's. Recently, excellent discrete HEMT's power performance has been reported. At 60 GHz, 1 W/mm with 2.9-dB gain, 25% power-added efficiency [1] and 0.83 W/mm with 4.5-dB gain and 32% power-added efficiency [2] have been obtained for small gate width HEMT's. The highest power output reported for a single discrete HEMT in this frequency range was 184 mW with 4.6-dB gain and 25% power-added efficiency at 55 GHz [3].

Even though these discrete HEMT's results are impressive, little work has been reported for high-gain, high-power, and high-efficiency MMIC amplifiers at this frequency. This letter presents the development of V-band MMIC power amplifiers with state-of-the-art performance. For a single-stage MMIC amplifier employing a 200-μm pseudomorphic HEMT (PHEMT), 151.4-mW output power with 26.4% power-added efficiency has been achieved at 60 GHz. The highest power-added efficiency achieved was 30.6% with 130 mW output power. A three-stage MMIC amplifier employing three 200-μm PHEMT's has achieved 80-mW output power with 20.5% power-added efficiency and 17-dB associated gain at 57 GHz. The linear gain of the amplifier was measured as high as 21.5 dB.

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II. MMIC Design

Millimeter-wave monolithic integrated circuits design is a technical challenge. Designing a V-band MMIC power amplifier requires the proper selection of devices as well as circuit topologies.

Device selected for V-band power amplifier was a PHEMT with a total gate periphery of 200 μm (8 $\times$ 25 μm). The gate length is 0.2 μm. The device's equivalent circuit model was derived from on-wafer S-parameter data measured from 0.045 to 40 GHz. From the equivalent circuit model, maximum available gain is calculated to be 8 to 9 dB at 60 GHz. The current gain of the devices was obtained from the S-parameters and the f_T was determined by extrapolating the frequency dependence of h_{21}. The device's f_T was 65 to 70 GHz when biased at V_D = 3 V and $I_D = \frac{1}{2}I_{\text{sat}}$The peak f_T appeared to be 80–90 GHz when biased at V_D = 1.2 V.

We used the same 200-μm PHEMT for the single-, two-, and three-stage MMIC amplifiers to ensure the first pass success. Fig. 1 shows the photograph of a fabricated three-stage MMIC amplifier. The dimensions of the chip are 1 $\times$ 3 mm. We chose microstrip transmission line based matching circuits to minimize the circuit loss and allow a simple structure for implementation. A series inductance and a shunt capacitance (open stubs) were used to form a resonate circuit to transform the device's input and output impedance to 50 ohms. The interstage matching was implemented by using a low-impedance transmission line. MIM capacitors were used for RF-bypass and dc-blocking application while thin-film resistors were used in the biasing networks to provide low-frequency stability. All grounding was achieved through via holes.

III. MMIC Fabrication

The device epi-structure utilized in this work is a double-sided δ-doped AlGaAs–InGaAs–GaAs PHEMT, as shown in Table I. The structure was grown by MBE on a GaAs substrate in a Varian GEN II system. A sheet charge density of over 3.2 $\times$ 10^{12}cm^{-2} and room temperature carrier mobility of 6000 cm^2/V-sec in InGaAs channel were measured. The gate-contact AlGaAs layer was undoped so that high gate-drain breakdown voltage can be achieved.

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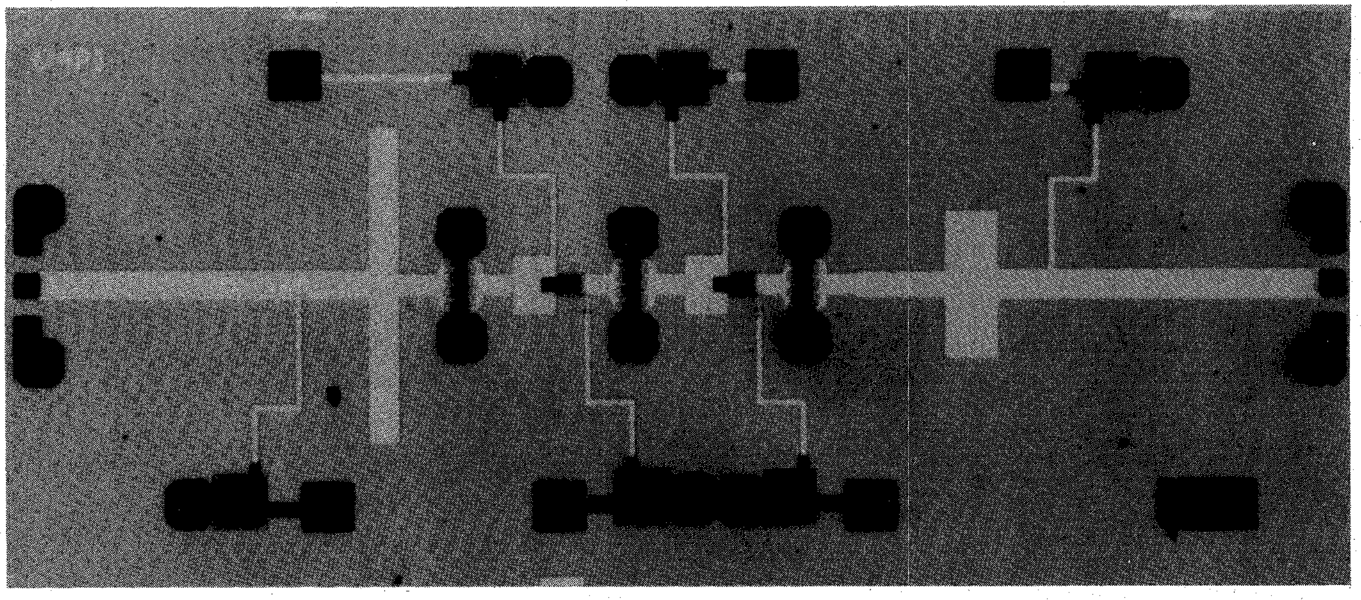

Fig. 1. V-band three-stage MMIC power amplifier.

TABLE I
DEVICE STRUCTURE OF A DOUBLE-SIDED δ-DOPED PHEMT

GaAs	CAP	2×10^{18} cm^{-3}	300 Å
$Al_{0.25}Ga_{0.75}As$	Schottky	2×10^{17} cm^{-3}	300 Å
Si Planar Doping		4-5 $\times 10^{12}$ cm^{-2}	
$Al_{0.25}Ga_{0.75}As$	Spacer	Undoped	25 Å
$Al_{0.20}Ga_{0.80}As$	Channel	Undoped	120 Å
GaAs	Spacer	Undoped	50 Å
Si Planar Doping		1×10^{12} cm^{-2}	
GaAs	Buffer	Undoped	
GaAs	S. I. Substrate		

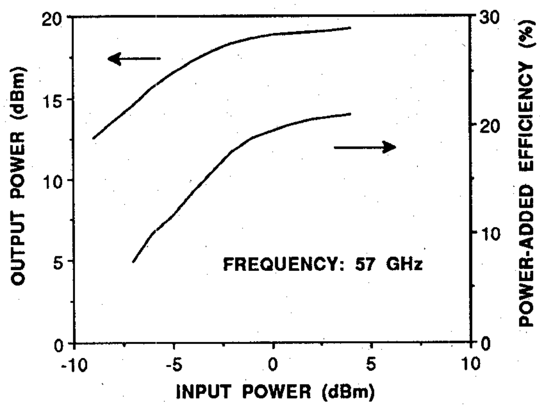

Fig. 2. Power performance for a V-band three-stage MMIC amplifier.

We utilized low-contact resistance AuGe based alloyed ohmic contact for both source and drain formations. We employed low-resistance mushroom gates. The gates were defined in PMMA/PMAA bilayer resist by E-beam lithography using a Phillips Beamwriter machine. After gate recess etching, a Ti–Pt–Au metal system was evaporated onto the gate opening region and lifted-off to form gate fingers.

Other MMIC components fabricated including TaN resistors, Ti–Au overlays (for both transmission line and capacitor's bottom metal), dielectric capacitors, top metal and Au-plated airbridge. After completing front-side processing, we then flipped the substrate over, thinned it down to 4 mils, RIE etched via holes and metalized the backside with Au. The fabricated PHEMT's exhibited a high full-channel drain current density ($I_{\max}$) of 650–700 mA/mm and a large transconductance (g_m) of 500–600 mS/mm. The typical source-drain breakdown voltage was 9 V and threshold voltage was −0.5 to −1.0 V.

IV. RF PERFORMANCE

Before dicing the wafer, we measured on-wafer small-signal performance of the amplifiers using an automated network analyzer for the frequency range from 30 to 60 GHz. A small signal gain of more than 10 dB from 52 to 60 GHz with a peak gain of 15 dB at 58 GHz was achieved for the two-stage amplifier and more than 20-dB gain was measured for the three-stage amplifier. The amplifier chips were then diced and mounted in a V-band test fixture for power test. The fixture utilized E-plane probe transitions to couple the RF power from microstrip lines to waveguides. The transition loss was measured to be approximately 0.5 dB at 60 GHz. Without any external tuning, we achieved 130 mW output power (650 mW/mm) with 30.6% power-added efficiency, and 151.4 mW output power (757 mW/mm) with 26.4% power-added efficiency at 60 GHz for a single-stage amplifier. For the three-stage amplifier, we achieved 80 mW output power with 20.5% power-added efficiency and 17-dB associated gain at 57 GHz, as shown in Fig. 2. These results, to our knowledge, set the state-of-the-art for V-band MMIC amplifiers.

V. CONCLUSION

We have successfully demonstrated a single-stage MMIC amplifier with 151.4 mW output power and 26.4% power-added efficiency at 60 GHz. The highest power-added efficiency achieved was 30.6% with 130 mW output power. For a three-stage MMIC amplifier employing the same devices, we achieved 80 mW output power with 20.5% power-added efficiency and 17 dB gain at 57 GHz. The performance can be further improved by optimizing the material structure and device size. This work demonstrates the potential of MMIC technology in the power areas for future millimeter-wave system applications.

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